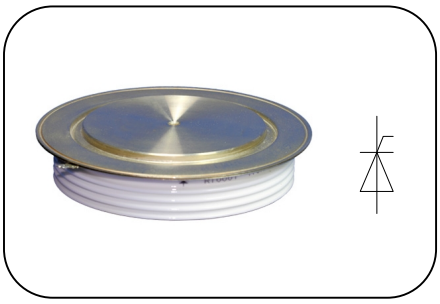


Features

- **n** Interdigitated amplifying gates
- **n** Fast turn-on and high di/dt
- **n** Low switching losses

Typical Applications

- **n** Design for inverter supply application

Part No. Y70KFG-KT60c(d)T	
$I_{T(AV)}$	**2206A**
V_{DRM}	**2000V~3000V**
V_{RRM}	**1000V~2500V**
t_q	**20~75μs**

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		T_j(°C)	VALUE			UNIT
					Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled,	T_C=55°C	125			2608	A
			T_C=70°C				2206	
V_{DRM}	Repetitive peak off-state voltage	tp=10ms		125	2000		3000	V
V_{RRM}	Repetitive peak reverse voltage				1000		2500	
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}		125			200	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}		125			28	kA
I^2t	I^2T for fusing coordination						3920	A^2s*10^3
V_{TO}	Threshold voltage			125			1.21	V
r_T	On-state slop resistance						0.16	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=4000A, F=32kN	20≤tq≤45	25			2.60	V
			46≤tq≤60				2.40	V
			61≤tq≤75				2.20	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=0.67V_{DRM}		125			1000	V/μs
di/dt	Critical rate of rise of on-state current	V_{DM}= 67%V_{DRM} to3000A Gate pulse t_r ≤0.5μs I_{GM}=1.5A		125			1500	A/μs
Q_{rr}	Recovery charge	I_{TM}=2000A, tp=4000μs, di/dt=-20A/μs, V_R=100V		125		1200		μC
tq	Circuit commutated turn-off time	I_{TM}=2000A, tp=4000μs, V_R=100V dv/dt=30V/μs, di/dt=-20A/μs		100	20		**75**	μs
I_{GT}	Gate trigger current	V_A=12V, I_A=1A		25	45		300	mA
V_{GT}	Gate trigger voltage				0.9		4.5	V
I_H	Holding current				20		500	mA
I_L	Latching current						1000	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=67%V_{DRM}		125			0.3	V
$R_{th(j-c)}$	Thermal resistance Junction to case	At 180^0 sine, double side cooled Clamping force 40kN					0.012	°C /W
$R_{th(c-h)}$	Thermal resistance case to heat sink						0.003	
F_m	Mounting force				30		40	kN
T_{vj}	Junction temperature				-40		125	°C
T_{stg}	Stored temperature				-40		140	°C
W_t	Weight					880/ 1140		g
Outline	KT60cT;KT60dT							

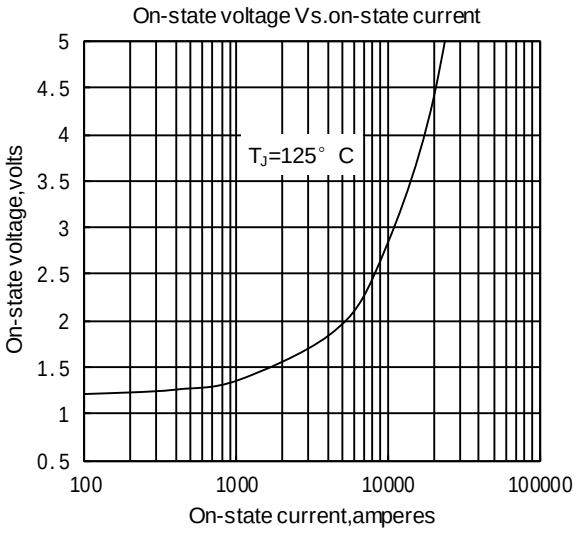


Fig.1

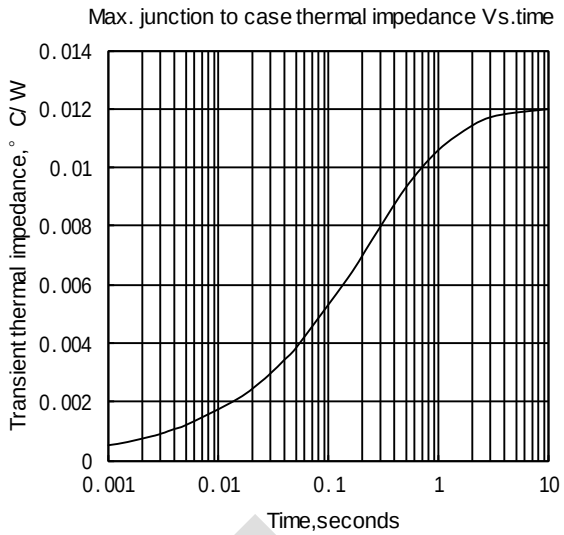


Fig.2

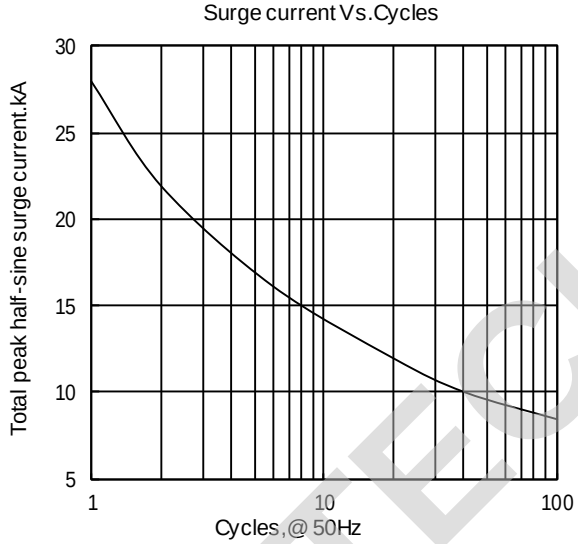


Fig.3

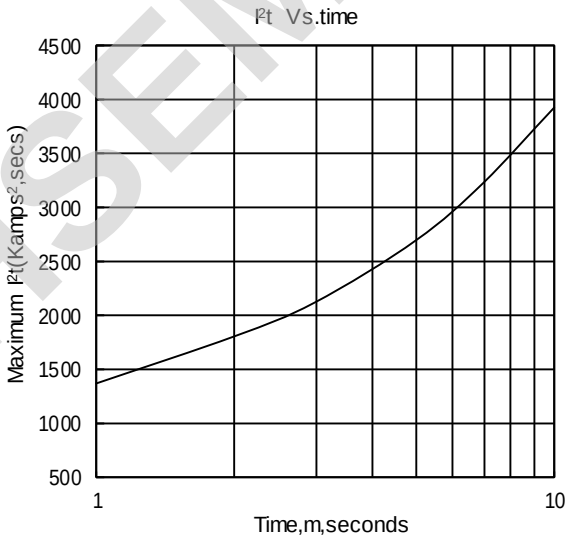


Fig.4

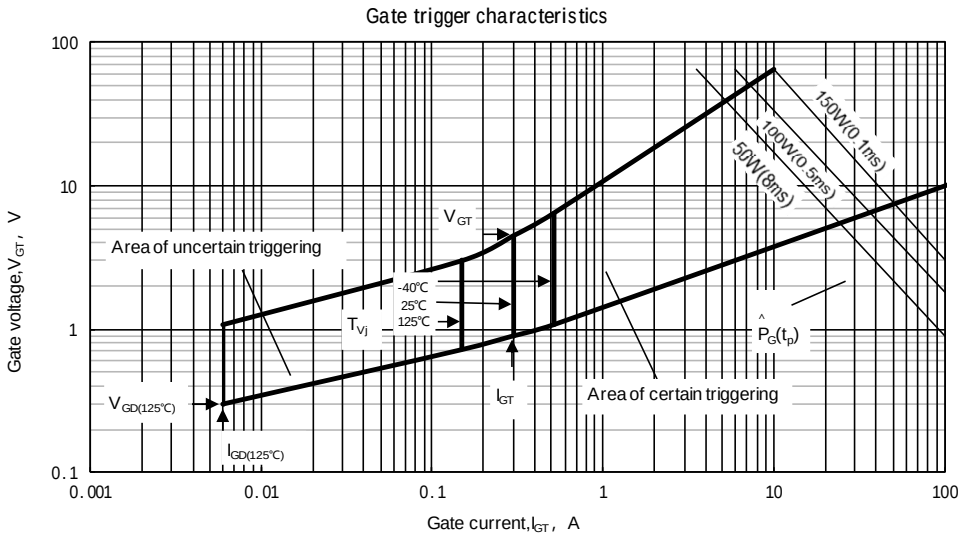
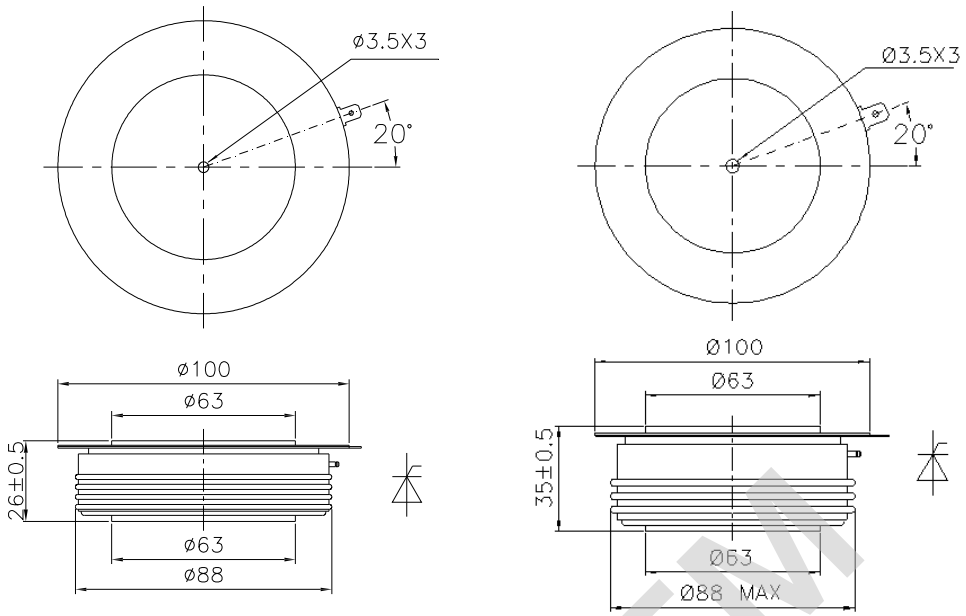


Fig.5

Outline:



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