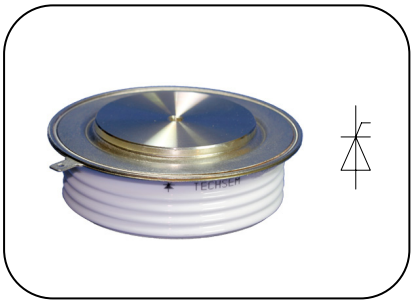
TECHSEM

Y50KPM
PHASE CONTROL THYRISTOR

Features:
- Center amplifying gate
- Metal case with ceramic insulator
- Low on-state and switching losses

Typical Applications
- AC controllers
- DC and AC motor control
- Controlled rectifiers

$I_{T(AV)}$	930A
V_{DRM}/V_{RRM}	4300-5200V
I_{TSM}	10 kA
I^2t	500 10^3A^2S



SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled, T_C=70°C	125			930	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	tp=10ms	125	4300		5200	V
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			120	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}	125			10	kA
I^2t	I^2t for fusing coordination					500	A^2s*10^3
V_{TO}	Threshold voltage		125			1.04	V
r_T	On-state slope resistance					0.84	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=1500A, F=24kN	25			3.20	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=0.67V_{DRM}	125			1000	V/μs
di/dt	Critical rate of rise of on-state current	V_{DM}= 67%V_{DRM} to1500A, Gate pulse t_r ≤0.5μs I_{GM}=1.5A Repetitive	125			100	A/μs
Q_{rr}	Recovery charge	I_{TM}=2000A,tp=2000μs, di/dt=-20A/μs, V_R =50V	125		1800		μC
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	40		300	mA
V_{GT}	Gate trigger voltage			0.8		3.0	V
I_H	Holding current			20		250	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=67%V_{DRM}	125	0.3			V
$R_{th(j-c)}$	Thermal resistance Junction to case	At 180° sine, double side cooled Clamping force 24kN				0.020	°C /W
$R_{th(c-h)}$	Thermal resistance case to heatsink					0.005	
F_m	Mounting force			19		26	kN
T_{stg}	Stored temperature			-40		140	°C
W_t	Weight				440		g
Outline	KT50cT						

On-state voltage Vs.peak on-state current

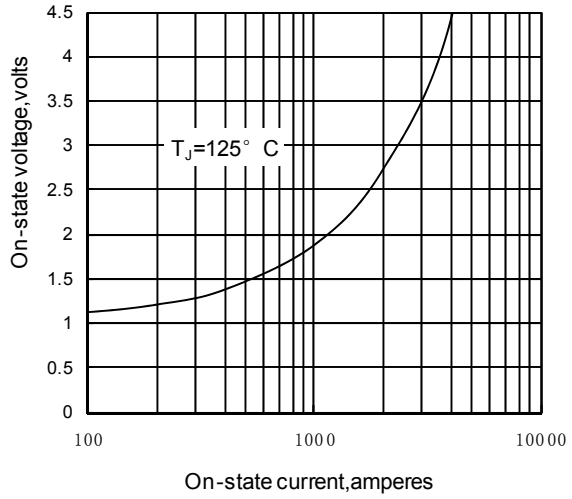


Fig1

Max. junction to case thermal impedance Vs.time

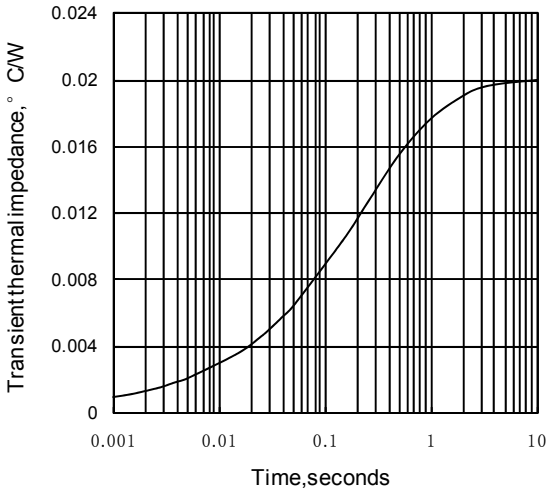


Fig2

Max. power dissipation Vs.mean on-state current

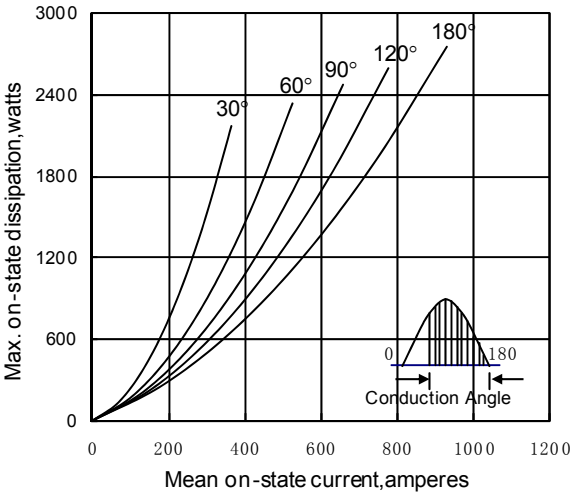


Fig3

Max.case temperature Vs.mean on-state current

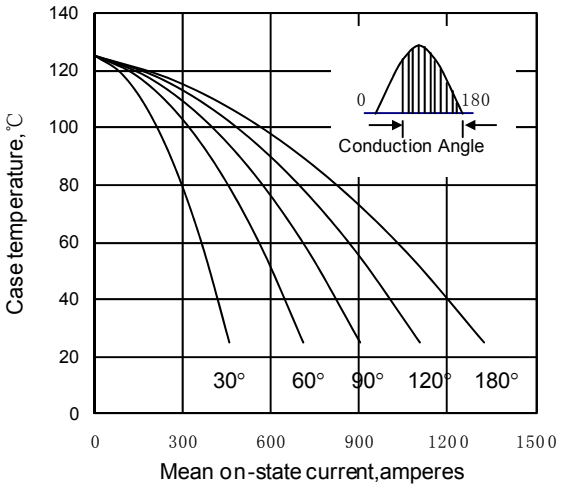


Fig4

Max. power dissipation Vs.mean on-state current

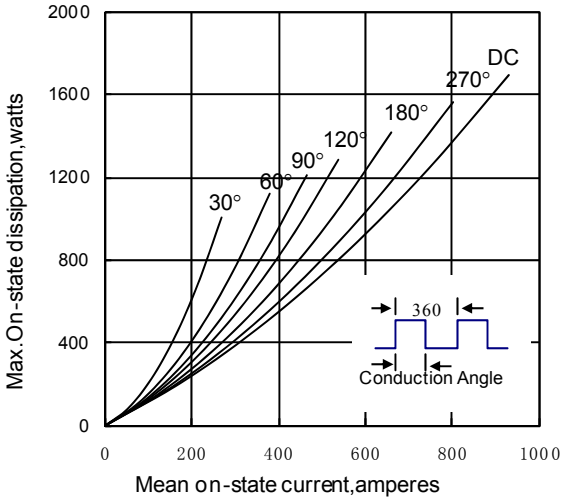


Fig5

Max. case temperature Vs.mean on-state current

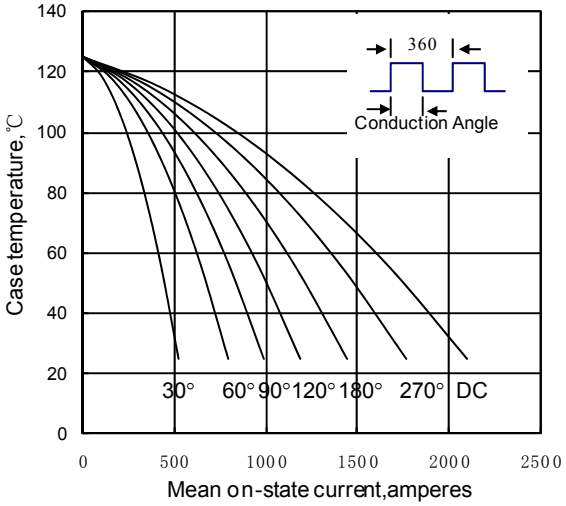


Fig6

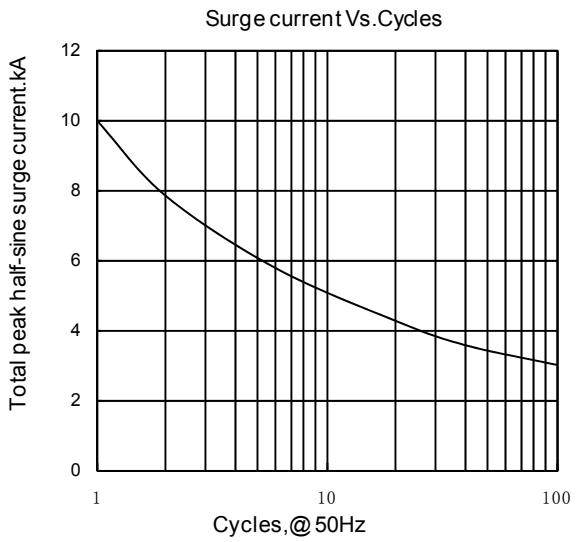


Fig7

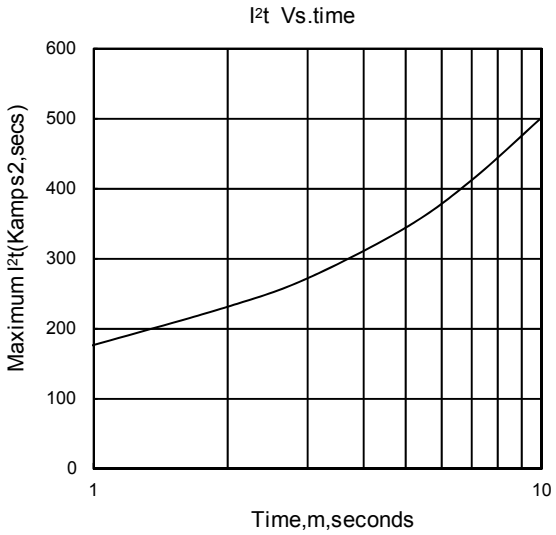


Fig8

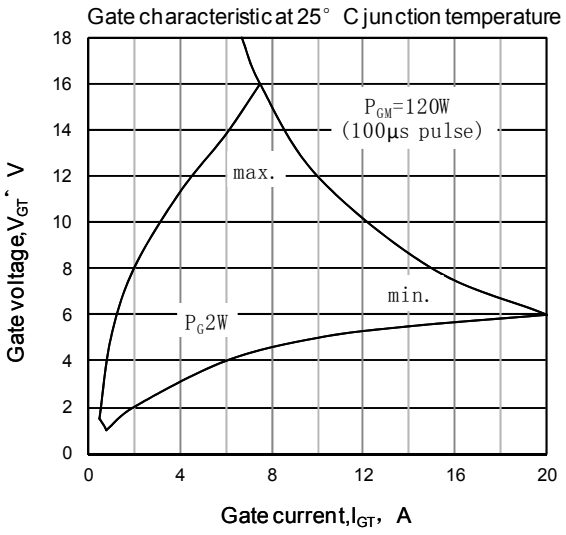


Fig9

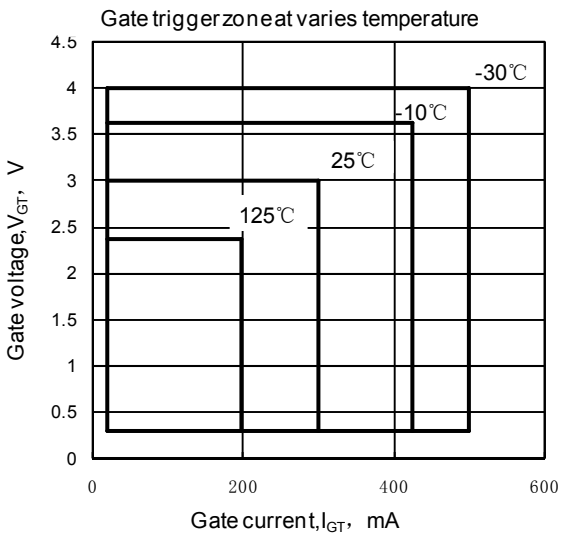


Fig10

Outline: